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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,365	12/12/2003	Chaur-Chin Yang	BHT-3183-63	8705
75	90 07/29/2005		EXAM	INER
BRUCE H. TF		•	PAREKH, NITIN	
SUITE 1404	AC DIVE		ART UNIT	PAPER NUMBER
5205 LEESBUR FALLS CHURG	CH, VA 22041		2811	
		DATE MAIL ED: 07/29/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

		M				
,	Application No.	Applicant(s)				
	10/733,365	YANG ET AL.				
Office Action Summary	Examiner	Art Unit				
	Nitin Parekh	2811				
The MAILING DATE of this communi Period for Reply	ication appears on the cover sheet w	ith the correspondence address				
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNI - Extensions of time may be available under the provisions after SIX (6) MONTHS from the mailing date of this community of the period for reply specified above is less than thirty (30). If NO period for reply is specified above, the maximum states a Failure to reply within the set or extended period for reply Any reply received by the Office later than three months a earned patent term adjustment. See 37 CFR 1.704(b).	CATION. of 37 CFR 1.136(a). In no event, however, may a unication. o) days, a reply within the statutory minimum of thi ututory period will apply and will expire SIX (6) MO will, by statute, cause the application to become A	reply be timely filed rly (30) days will be considered timely. NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) file	d on <u>25 May 2005</u> .					
2a)⊠ This action is FINAL.	This action is FINAL . 2b) ☐ This action is non-final.					
,] Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practic	ce under <i>Ex parte Quayle</i> , 1935 C.I). 11, 453 O.G. 213.				
Disposition of Claims						
4) Claim(s) 1 and 2 is/are pending in th	e application.					
4a) Of the above claim(s) is/ar	e withdrawn from consideration.					
5) Claim(s) is/are allowed.	Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1 and 2</u> is/are rejected.	Claim(s) <u>1 and 2</u> is/are rejected.					
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restric	tion and/or election requirement.					
Application Papers						
9)☐ The specification is objected to by the	e Examiner.					
10)⊠ The drawing(s) filed on 12 December	<u>2003</u> is/are: a)⊠ accepted or b)[☐ objected to by the Examiner.				
Applicant may not request that any object	ction to the drawing(s) be held in abeya	nce. See 37 CFR 1.85(a).				
Replacement drawing sheet(s) including	the correction is required if the drawing	g(s) is objected to. See 37 CFR 1.121(d).				
11)☐ The oath or declaration is objected to	by the Examiner. Note the attache	d Office Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim (a) All b) Some * c) None of:		§ 119(a)-(d) or (f).				
1. Certified copies of the priority						
	documents have been received in A					
	of the priority documents have been	received in this National Stage				
* See the attached detailed Office action	nal Bureau (PCT Rule 17.2(a)).	t received				
See the attached detailed Office action	n for a list of the certified copies no	. receiveu.				
Attachment(s)	4) T Internite	Summary (PTO 412)				
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (P 	TO-948) Paper No	Summary (PTO-413) (s)/Mail Date				
3) Information Disclosure Statement(s) (PTO-1449 or Paper No(s)/Mail Date		Informal Patent Application (PTO-152)				

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DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. 5903052) in view of Paniccia (US Pat. 5895972).

Regarding claims 1 and 2, Chen et al. disclose a BGA type/conventional thin-type BGA semiconductor package (see 10 in Fig. 1) comprising:

- a composite multilayered substrate (CMLS)/printed wiring board substrate
 (PWBS) including a MLS/PWB (see 24/12a/12b in Fig. 1) and a heat
 spreader/heat slug (HS-16 in Fig. 1),
- the MLS/PWB having an upper surface, a lower surface and an opening (see
 26/12e in Fig. 1), the opening passes through the upper surface and the lower
 surface, a step is formed in the opening (see Fig. 1)
- the HS has a first/top surface and a second/bottom surface where the first surface is attached to the lower surface of the MLS/PWB
- a plurality of ball pads (36/34 in Fig. 1) are formed on the lower surface, a plurality of bonding sites/connecting pads are formed on the step (not numerically

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referenced in Fig. 1; see bonding wire connections on the surface 12a in Fig. 1; Col. 4, lines 14-20) and electrically connect with the ball pads

- the HS being attached to the lower surface of the MLS/PWB and covers the opening to form a chip cavity
- an integrated circuit (IC) chip (14 in Fig. 1) disposed in the chip cavity, the chip having an active/upper surface and a back/lower surface
- a plurality of bonding pads being formed on the active surface and electrically connected to the connecting pads of the wiring board (see Fig. 1), the back surface of the chip being attached to the HS
- a package body comprising an encapsulate/dispensing material/sealant (30 in Fig. 1) being formed in the chip cavity of the composite substrate sealing the IC chip and bonding wires (see 30, 14 and 20 respectively in Fig. 1)
- a plurality of solder bumps/balls (22 in Fig. 1) on the ball pads
- the HS having a thickness being smaller than the height/diameter of the solder bumps/balls (see Fig. 1 and 5), and
- the HS having an exposed lower surface opposing the surface being attached to the MLS/PWB, a solder/metal (see 44 at the lower surface of 16 in the final structure of Fig. 5; Col. 4, lines 30-46) film being formed on the exposed surface
 (Fig. 1-5; Col. 2, line 45- Col. 4, line 46)

Chen et al. disclose the HS being attached to the back/lower surfaces of the chip and the MLS/PWB wherein the HS has the metal film over the second surface, but fail to teach a dummy die being attached to the lower surfaces.

Paniccia teaches a thermally dissipative wire bonded package having a heat slug (HS) being attached to a back surface of a device/chip (see 820 and 802 respectively in Fig. 9A) wherein the HS comprises a dummy substrate without any electrical connections therein, such dummy silicon die substrate (820 in Fig. 9A) providing the desired thermal performance for the device application requirement (Col. 8, lines 1-20; Col. 5, lines 57-63).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the dummy die having the metal film on the second surface being attached to the lower surfaces of the chip and the wiring board as taught by Paniccia so that the desired thermal dissipation can be achieved in Chen et al's BGA.

Response to Arguments

- 3. Applicant's arguments filed on 05-25-05 have been fully considered but they are not persuasive.
- A. Applicant contends that Paniccia does not teach the composite substrate and the dummy die having the metal film.

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However, the primary reference of Chen et al. discloses the BGA structure comprising the CMLS and the HS having the metal film. Paniccia is combined with Chen et al. to provide the dummy die under the chip to improve the heat dissipation.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

NITIN PAREKH

NtisPareth

07-27-05

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800